Fall 2017 Mid-Exam（答案卷） RTS

Name:_______________ Score:__________

ID:_________________

Read each question over carefully several times. Answer all questions in the space provided. The exam is 150minutes long. The total score is 104.

(1). Please define the following terminologies (12pts):

a. Time Redundancy in Real-Time Fault Tolerance

(3) Masking fault by repetition of a computation or communication

b. Dynamic Voltage Scaling

(3) Dynamic increasing/decreasing of the supply/operating voltage (1) of a processor allows operation at a higher/slower speed (1) with more/less energy consumption (1).

c. Power Supply Gating

(3) Cut off the power supply to inactive (1) units/components to reduce the leakage (2).

d. 3-Partition Problem

(3) $A = \{a_1, a_2, \ldots, a_{3m}\}$, B a positive integer, and $w_1, w_2, \ldots, w_{3m}$ be integral weights of elements of A, respectively such (1) that $B/4 \le w_i \le B/2$, and the sum of w_i is equal to mB. The decision is whether A can be partitioned into m disjoint sets such that each of which has weight B. (2)

(2) Please compare the Earliest Deadline First Algorithm (EDF) and the Least Slack Time Algorithm (LST) in terms of the Least Upper Bound of Utilization Factor when the context switch cost can be ignored. If the context switch cost can not be ignored, please compare the comment on the impacts on the calculation of their Least Upper Bound of Utilization Factor. (10pts)

Ans: (2) LST and EDF (2) both has the bound as 100% if the context switch cost can be ignored. If not, the bound of LST can be far less than that of EDF because of the context switch number can be proportional to the value of the maximum task period in the worst case (3) under LST, but the EDF only has two context switches for each task execution. (3)

(3) Please explain the relationship between (the definitions of) the Critical Instant and (the definitions of) the Fully Utilization of the Processor Power. Please explain the relationship between (the definitions of) the Fully Utilization of the Processor Power and (the definition of) the Least Upper Bound of the Utilization Factor. (12pts)

Ans: The processor is fully utilized when we can no longer increase the execution time of any task when it runs at its Critical Instant. The Least Upper Bound of the Utilization Factor is the minimum utilization factor of all tasks that fully utilize the processor.

(4) Priority Inversion must be managed so as to guarantee the schedulability of real-time processes. Please comment on the impacts on the worst-case Priority Inversion number and time and the possibility of a deadlock when we remove Priority Inheritance from the Priority Ceiling Protocol Please comment on the impacts on the worst-case Priority Inversion number and time and the possibility of a deadlock when we adopt Priority Inheritance for the Highest Locker's Priority. What would we do if a task might suspend itself after it locks a semaphore and enters its critical section under the Priority Ceiling Protocol and why? And what will happen when you do so? (20pts)

Ans: (1) No deadlock, Still one priority inversion, potentially longer priority inversion time (2) No change… No deadlock, Still one priority inversion, same worst-case priority inversion time (3) A locked semaphore should be released because the long blocking time might prevent the system from granting any semaphore to any task. The problem is no protection over data or potential roll back if any conflict happens.

(5) Please compare EDF and the Rate Monotonic Scheduling Algorithm (RMS) in terms of the least upper bound of the utilization factor, transient overloading, its implementation over a common operating systems such as Linux with fixed-priority levels. (9pts)

Ans: (a) EDF: 100%, RMS: $m(2^{1/m}-1)$; (b) RMS has stability property, where EDF might keep executing the to-miss-deadline tasks. (c) EDF might have priority shuffling in keep reassigning tasks priorities. RMS ~ no extra cost

(6) Under the Priority Ceiling Protocol, please prove why there is no chain blocking. (10pts)

Ans: Proof sketch: no hold and wait.

(7) Why the Deadline Modification algorithm is a pseudo-polynomial algorithm? Given N processes, suppose that processes are given the processor time in an uninterruptible quantum, say q. Suppose that there are M mini scheduling blocks in the interval $[0, L]$ where $L = \text{LCM}(p_i)$. What is the maximum number of forbidden regions? Why? (10pts)

Ans: (a) It is because the complexity of the algorithm might be the function of the maximum value of the periods. (b) M

(8) Please explain why parallelism could save energy. (6pts)

Ans: It is because we can have the concurrrent execution of subtasks of a task over multiple cores, and the energy consumption function and the supply voltage has the following relationship:

$$E \propto V_{dd}^2 (\#\text{cycles})$$

$$E_2 = \frac{1}{4} E_1$$

(9). RMA: Consider the following process set with the assigned priorities (Max:1, Min:4): (hint: use schedulability bound tests, completion time test, or schedulability point test. All critical sections are NESTED.) (15pts)

	T1	T2	T3	T4
Pi	50 (periodic)	120 (periodic)	210 (periodic)	300 (periodic)
Ci	10	30	60	60
Semaphores	S1(5)	S1(10)	S1(15),S2(20)	S2(20)
deadline	50	90	180	300
priority	2	1	4	3

(a) Consider periodic process set {T1, T2, T3, T4} without semaphore sharing and without pre-period deadlines. Show me which process is schedulable or unschedulable.

(b) Consider periodic process set {T1, T2, T3, T4} without semaphore sharing but with pre-period deadline. Show me which process is schedulable or unschedulable.

(c) Consider periodic process set {T1, T2, T3, T4} with semaphore sharing and pre-period deadline. Show me which process is schedulable or unschedulable under the Priority ceiling Protocol..

(a)
T1: 10+30 < 50 ....(S)
T2: 30 < 120 ...(S)
T3: 60+5*10+2*30+60 > 210 ...(U)
T4: 60+6*10+3*30 < 300 ...(S)
.
(b)
T1: 10+30 < 50 ...(S)
T2: 30 < 90 ...(S)
T3: 60+4*10+2*30+60 > 180 ...(U)
T4: 60+6*10+3*30 < 300 ...(S)
.
(c)
T1: 10+30+15 > 50 ...(U)
T2: 30+15 < 90 ...(S)
T3: 60+4*10+2*30+60 > 180 ...(U)
T4: 60+6*10+3*30+20 < 300 ...(S)